

## Smart Processor Picks for Consumer Media Applications

*Optimized DSP Software • Independent DSP Analysis*



### Smart Processor Picks for Consumer Media Applications (Workshop 246)

Berkeley Design Technology, Inc.  
2107 Dwight Way, Second Floor  
Berkeley, California 94704  
USA  
+1 (510) 665-1600

info@BDTI.com  
<http://www.BDTI.com>

© 2003 Berkeley Design Technology, Inc.



### Outline

- Motivation and scope
- Application structure and requirements
- Challenges
- Processor architecture options
- Selection methodology
- Conclusions

© 2003 Berkeley Design Technology, Inc.

2

© 2003 Berkeley Design Technology, Inc.



## Outline

- **Motivation and scope**
- Application structure and requirements
- Challenges
- Processor architecture options
- Selection methodology
- Conclusions

© 2003 Berkeley Design Technology, Inc.

3



## Motivation

- Technology creates new opportunities, e.g.,
  - Broadband internet enables video on demand
  - Low-bit rate voice codecs enable all-digital voice recorders
- “Right” processor key to product success
  - Supports, enables, desired product features
  - Defines product performance (end user experience)
  - Can simplify development effort and cost
- Range of processor options is large, dynamic, growing, making selection difficult

© 2003 Berkeley Design Technology, Inc.

4



### Scope

- Processor selection for consumer media products with varying features:
  - Application a mix of audio, video, or still image
    - MP3 players, voice recorders, cell phones
    - Still or video cameras, photo picture frames
  - Using streaming or stored content
  - Battery or line powered, portable or fixed
  - Low or high cost (relative, to consumers)
  - Input/output quality varies by application
    - E.g., lower quality audio for voice recorder, high quality audio for MP3 or DTS playback

© 2003 Berkeley Design Technology, Inc.

5

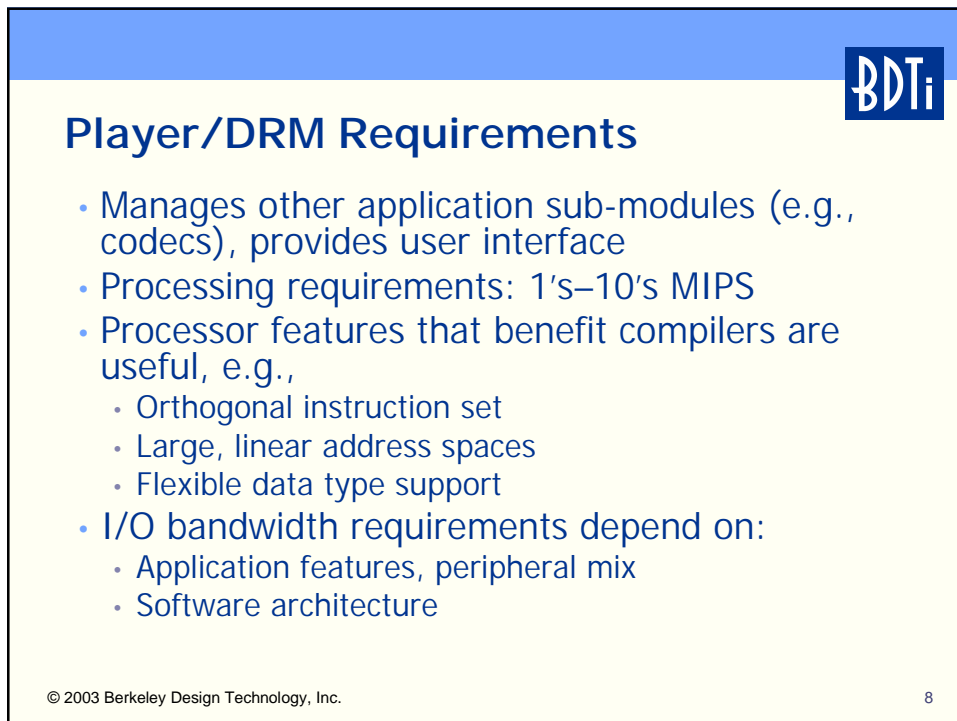
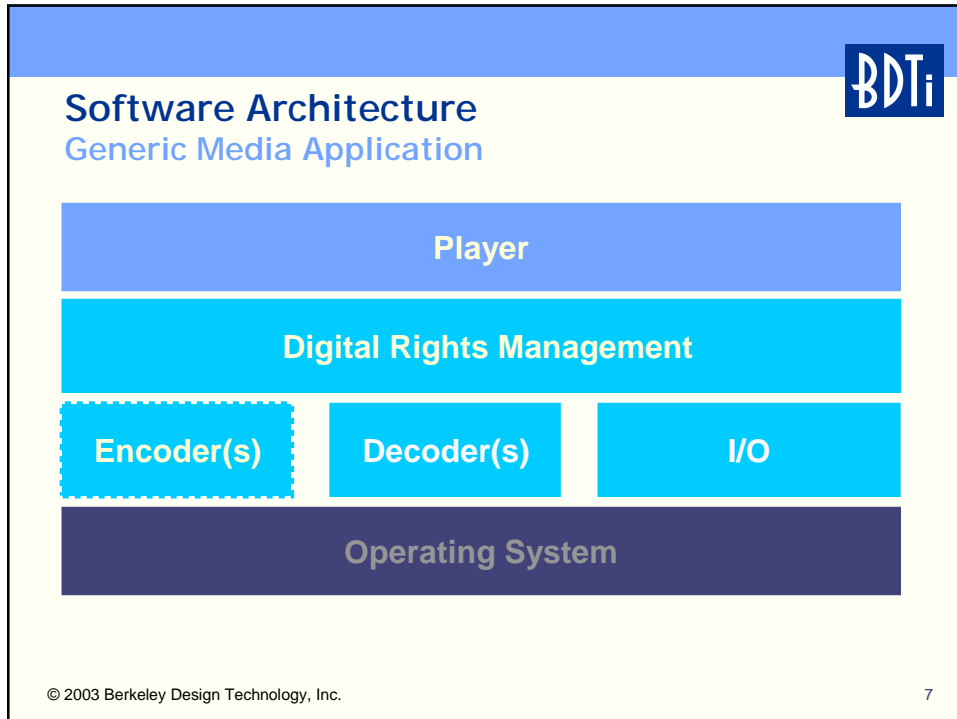


### Outline

- Motivation and scope
- **Application structure and requirements**
- Challenges
- Processor architecture options
- Selection methodology
- Conclusions

© 2003 Berkeley Design Technology, Inc.

6





## Audio Codec Requirements

- Memory requirements moderate
  - Audio data rates 1's–100's KB/s
  - Data working set size per frame small (few KB)
  - Codec memory footprint on order of 10's KB
- Processor power required: 1's–10's MIPS
- Data types depend on application
  - Music applications need higher fidelity than speech (wider words, in general)
- Post-processing may be required
  - E.g., sample rate conversion, mixing

© 2003 Berkeley Design Technology, Inc.

9



## Video Codec Requirements

- Memory requirements high
  - Data rates 10's–1,000's of KB/s
  - Working data sets 10's–100's of KB
  - Memory footprints typically 10's–low 100's KB
- Processing power required: 10's–100's MIPS
- Typically, 8- or 16-bit data types sufficient
  - Latency, throughput more important
- Post-processing of frames may be required
  - Alpha blending, color conversion, scaling, ...

© 2003 Berkeley Design Technology, Inc.

10



### I/O Requirements

- Integrated I/O is an advantage
  - Basic serial & parallel (SPI, "host port")
  - Advanced standards (Ethernet, ATA, USB, 1394)
  - Memory ports (e.g., glueless SDRAM, wireless, smart cards)
- Autonomous, intelligent I/O is even better
  - E.g., programmable communications co-processors reduce load on core processor
- Development effort
  - Peripheral programming model complexity
  - Off-the-shelf device drivers, OS support
  - Support for I/O in debug, development tools

© 2003 Berkeley Design Technology, Inc.

11



### Operating System Requirements

- OS functions command & control oriented
  - E.g., inter-task communication, scheduling
- OS overhead generally low: require few MIPS
  - Memory footprint can be large—and problematic
- Availability important, and how available
  - E.g., player, DRM, may be tied to specific OS
  - OS easier to customize if available as source
  - Cost and support issues
- To obtain good OS performance, useful processor features include:
  - Good interrupt & context switch support, low latency
  - Memory management capabilities and large address space

© 2003 Berkeley Design Technology, Inc.

12



### Outline

- Motivation and scope
- Application structure and requirements
- **Challenges**
- Processor architecture options
- Selection methodology
- Conclusions



### Processor Selection Challenges

The fundamental problem:

- Many processors to choose from
- Complex processors, applications
- Many important selection criteria to consider
- Unpredictable dynamism in processor options, application requirements
- Poor information, complex analysis
- Limited time and resources for selection

The wrong choice can be fatal for a product development effort

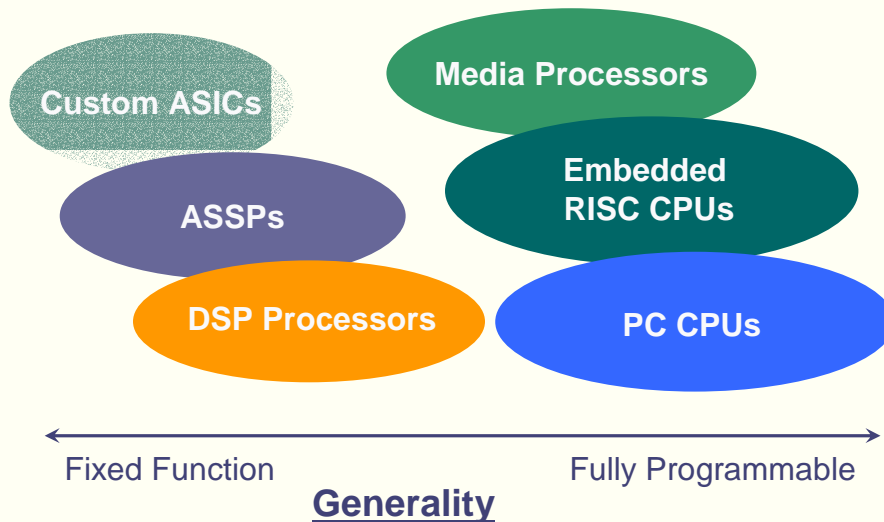


## Outline

- Motivation and scope
- Application structure and requirements
- Challenges
- **Processor architecture options**
- Selection methodology
- Conclusions



## Processor Categories







## ASICs

### Strengths and Weaknesses

- ↑ Offers the ultimate in tailored hardware
  - ↑ Speed, energy efficiency, cost/performance, ...
  - ↑ Integration to match the product requirements
  - ↓ Design usually inflexible
- ↓ Large development costs and risks vs. off-the-shelf hardware; NRE \$ increasing
  - ↓ Iteration is costly and time consuming
  - ↓ Lengthy development cycles
- ↓ Hardware/software integration and whole-chip testing are particularly challenging
  - ↓ Hardware/software partitioning typically must be done early
- ↓ Complex, costly, unreliable tools
- ↑ Vast architectural options

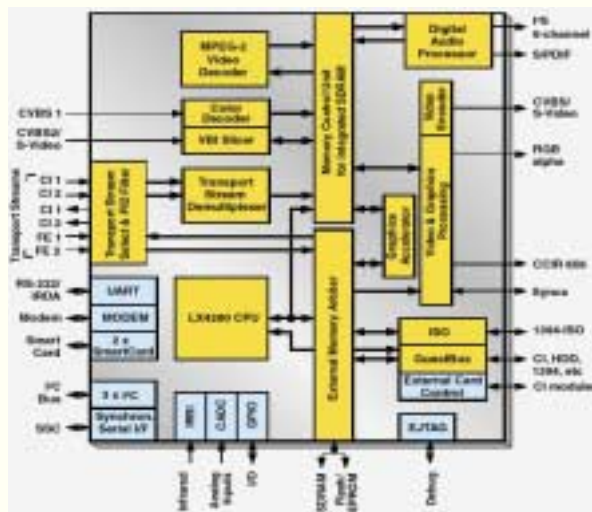
© 2003 Berkeley Design Technology, Inc.

17



## Example ASSP: Micronas MDE9500

- High-integration digital TV receiver
- Analog decode, DVB decryption, decode
- On-chip MPEG-2 video decoder (D1, 30 fps)
- Interfaces to other chips for, e.g., PVR functionality
- Customizable via software
  - MIPS-compatible CPU
  - Supports DVB-MHB
  - Supports Java
- Price?



© 2003 Berkeley Design Technology, Inc.

18



## ASSPs

### Strengths and Weaknesses

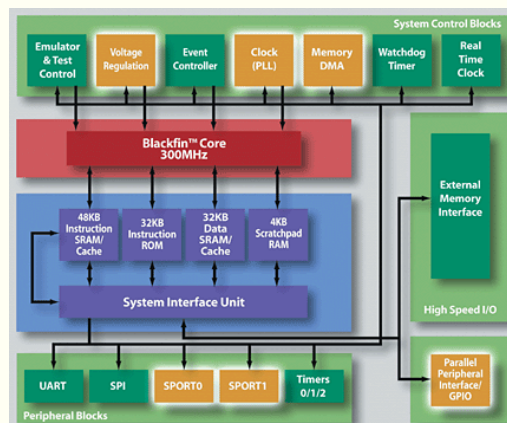
- ↑ Often very well matched to the application
  - ↑ SoCs with extensive integration
  - ↑ Architecture tuned for the application
  - ↑ Can yield excellent performance, cost, energy efficiency
- ↑ Ease of use
  - ↑ Reduce system development costs
  - ↑ Reduce required implementation expertise
- ↓ Often inflexible
- ↓ Limited differentiation opportunities for system designer
- ↓ Usually single-source
- ↓ Roadmap often unclear



## Example: DSP Processors

### Analog Devices Blackfin 21532

- Enhanced 300 MHz, 16-bit fixed-point DSP with dual-MAC units
- ADSP-2153x  
BDTImark2000™ score: 1,690
- Integrated peripherals target media apps (e.g., CCIR-656 port, I<sup>2</sup>S ports)
- Good 3<sup>rd</sup> party software component support
- MPEG-4 decode, simple profile, CIF: 168 MHz
- Price \$10, qty 10k





## DSP Processors

### Strengths and Weaknesses

- ↑ DSP performance, efficiency strong compared to other off-the-shelf processors
- ↓ But not as strong as customized solutions, and may not be adequate for demanding tasks
- ↑ DSP-oriented development tools, infrastructure
- ↓ Tools not as sophisticated as those available for general-purpose processors
  - ↓ Often, poor compiler quality
- ↑ Mature technology
- ↑ Third-party DSP application software available
  - ↓ Support for non-DSP software not as strong as, e.g., RISC
- ↑ Relatively low development cost, risk

© 2003 Berkeley Design Technology, Inc.

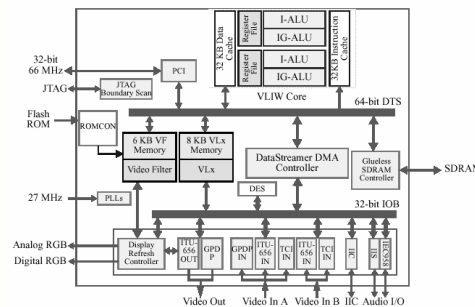
21



## Example: Media Processors


### Equator Technologies BSP-15

- General-purpose 400 MHz four-way VLIW, with extensive SIMD support
- On-chip L1 data, instruction caches
- Media-specific interfaces, co-processors
- C/C++ programming model
- Few software components available
- MPEG-4 decode (simple profile, CIF, 30 fps): 60 MHz
- Price believed to be ~\$40



© 2003 Berkeley Design Technology, Inc.

22




## Media Processors

### Strengths and Weaknesses

- ↑ Higher performance than most DSPs, GPPs
  - ↑ VLIW, huge register sets, wide SIMD typical
  - ↑ High performance peripherals, co-processors
- ↓ Very complex programming models
- ↑ Better DSP support in development tools, infrastructure, compared to GPPs
- ↓ Application performance compiler-dependent
  - ↓ Compilers can be poor quality
- ➔ Maturing technology—but roadmaps unclear
  - ↓ 3<sup>rd</sup> party support weaker than other CPU types
- ↑ Development cost, risk, lower than ASIC

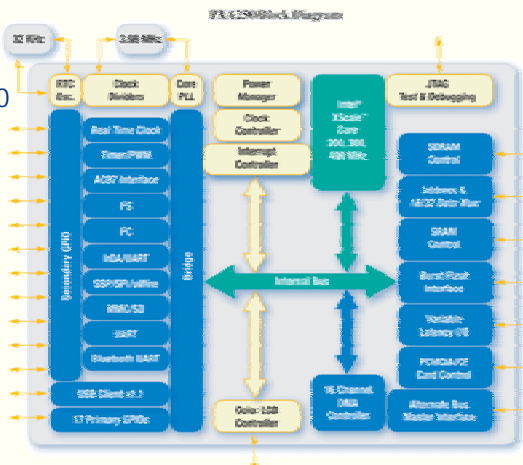
© 2003 Berkeley Design Technology, Inc. 23



## Example: Embedded RISC CPU

PXA250

- 400 MHz, 32-bit RISC with modest DSP extensions
- BDTIMark2000™ score: 930
- MPEG-4 decode (simple profile, CIF @ 30 fps) 200-240 MHz
- 16-bit SIMD, 32-bit data types benefits media apps
- Predicated instruction execution good for control
- Good development tool support, optimized DSP software available (e.g., Intel IPP)
- Price \$37.30, qty 10k



PXA250 Block Diagram

© 2003 Berkeley Design Technology, Inc. 24



## Embedded RISC CPUs

### Strengths and Weaknesses

- ↑ Can have strong DSP performance
- ↓ Dynamic features complicate programming
  - ↓ Complicates optimization & ensuring real-time
- ↓ Sometimes, convoluted programming model
- Good tools, but generally lack DSP support
- ↑ 32-bit GPPs better targets for non-DSP tasks
  - ↑ E.g., TCP/IP network stacks
- ↑ Multi-vendor architectures more common
- ↑ Very good third-party software component support
- ↑ Compatibility more common
- ↑ High integration parts increasingly common

© 2003 Berkeley Design Technology, Inc.

25



## Example: PC CPU

### VIA Technologies C3

- 1 GHz x86 compatible
- Moderate power consumption, cost
- SSE support for media applications, supports fixed-, floating-point types
- Access to massive x86 3<sup>rd</sup>-party software, tools base
- Familiar to software, hardware developers
- MPEG-2 decode (D1, 30 fps) using 5-15% of CPU, when using VIA Apollo CLE266 chipset
- CPU: \$39, chipset: \$23 (qty 10k)

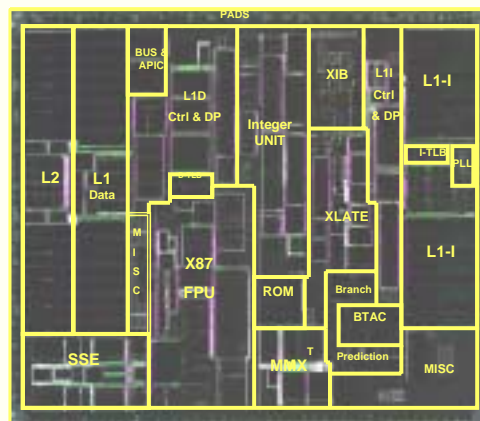


Image © VIA Technologies

© 2003 Berkeley Design Technology, Inc.

26



### PC CPUs (GPPs)

#### Strengths and Weaknesses

- ↑ High-performance GPPs (e.g., Intel Celeron, VIA C3) can implement complex DSP tasks
  - ↑ May be as fast or faster than DSPs...
  - ↓ ...but cost & power consumption typically higher
- ↓ Dynamic features complicate optimization, real-time design
- ↑ Many options for OS, 3rd party application software
- ↑ Development tools mature, powerful
  - ↓ But typically lack features useful for media application development

© 2003 Berkeley Design Technology, Inc.

27



### Outline

- Motivation and scope
- Application structure and requirements
- Challenges
- Processor architecture options
- **Selection methodology**
- Conclusions

© 2003 Berkeley Design Technology, Inc.

28



## Processor Selection Methodology

Use a hierarchical approach to make the problem manageable:

- Determine selection criteria
- Prioritize or assign weights to selection criteria
- Use critical criteria to eliminate obviously unsuitable choices
  - Begin with classes of processors
- Evaluate and rank candidates
- Weigh trade-offs among non-critical criteria
- Iterate as necessary
  - Refine criteria and analysis of candidates

© 2003 Berkeley Design Technology, Inc.

29




## Processor Selection Criteria

### Signal-Processing-Centric Concerns

- Performance on relevant DSP tasks
  - Speed
  - Memory bandwidth: on-chip, off-chip
  - Execution-time predictability
    - Dynamic features confound determinism
  - Energy consumption
- Numeric fidelity, bit-exact standards
  - Fixed-point vs. floating-point
  - Data word size(s)
  - Support for extending precision
- Memory usage

© 2003 Berkeley Design Technology, Inc.

30



## Processor Selection Criteria

### Signal-Processing-Centric Concerns

- On-chip integration
  - Memory, peripherals, I/O interfaces, coprocessors
- Development effort, risk
  - DSP-oriented tools, infrastructure
  - Programming model complexity
  - Application software components
  - Tools, support (vendor, 3<sup>rd</sup> party)
  - Features useful for integration, real-time testing
    - E.g., on-chip debug support
  - Accurate cycle-count and memory profiling
  - Visibility into cache, pipeline

© 2003 Berkeley Design Technology, Inc. 31



## Processor Selection Criteria

### General Concerns

- Cost
- Packaging options
- Roadmap
  - Availability; reliability of supply
    - Multi-vendor architectures a plus
  - New spins, new architectures, compatibility
  - Core version available?
- Special requirements
  - Variable-voltage operation

© 2003 Berkeley Design Technology, Inc. 32





## Assessing Performance

- Use results from relevant application modules
  - More accurate than benchmark mapping—if available
  - Use caution! The data may be misleading or incomplete.
- Use benchmarks & application profile
  - Useful when application data isn't available
  - Uses kernel benchmark results to predict application module performance
- Use care with either approach
  - Hazards include data types, multitasking effects, ...

© 2003 Berkeley Design Technology, Inc.

33



## Assessing Performance, continued

- Core CPU performance isn't enough
  - Must also consider memory sizes and bandwidths
  - I/O bandwidths and overheads
- Impact of software partitioning in multi-processor systems
  - Must refine software architecture to predict performance
- Dynamic features complicate performance prediction
- Assessing energy efficiency can be very difficult

© 2003 Berkeley Design Technology, Inc.

34



## Other Development Considerations

- Language support
  - Quality of C compiler; availability of C++ compiler
  - Support for assembly language optimization
- Software availability
  - Player, device drivers, operating system
- Debug/development benefit from tools with:
  - Peripheral and multi-processor simulation
  - Non-intrusive, real-time debug
- Compatibility, developer familiarity

© 2003 Berkeley Design Technology, Inc.

35



## Availability and Roadmap

- Risk
  - Is the chip available in volume today?
  - Are there second sources of the chip, or compatible chips?
  - What does the errata list look like?
- Roadmap
  - What is the vendor's commitment to evolving the chip? E.g., improved integration, reduce cost
  - What is the vendor's roadmap for next-generation chips? Compatibility?
  - What is your confidence that the vendor will execute on its roadmap?

© 2003 Berkeley Design Technology, Inc.

36



### Outline

- Motivation and scope
- Application structure and requirements
- Challenges
- Processor architecture options
- Selection methodology
- **Conclusions**



### Conclusions

- Choosing a processor for a consumer media product is easy
- Choosing the *best* processor for your particular product is hard
  - Vast range of options
  - Many complex, competing criteria to consider
  - Poor information
  - Limited time and resources



### Conclusions, cont.

- Use a hierarchical approach
  - Develop a well-defined hierarchy of product requirements
  - Start with the critical criteria, and iteratively narrow the field
  - Expect to make trade-offs
- Assessing performance is a challenge
  - Resource-hungry algorithms, cost-constrained processors
- Development-related considerations are key
- Appropriate integration is essential to low system cost

© 2003 Berkeley Design Technology, Inc.

39



### Trends: Processors

- Consumer media applications are becoming a major focus of processor vendors
  - Expect more competitors, more options
- Technology, competition pushes performance up; price, power consumption down
  - Enabling new types of products, new levels of functionality
  - But not all processors are well matched to media processing workloads
- Increasing architectural complexity
  - Many heterogeneous multiprocessors
- Integration increasing
- Development infrastructure is a key differentiator

© 2003 Berkeley Design Technology, Inc.

40



### Trends: Development

- Products are becoming more complex
  - MP3 player vs. multimedia cell phone
- Processors are becoming more complex
- Algorithms are becoming more demanding
  - Nobody knows which ones will dominate
- Optimization continues to be essential
- Huge processor-to-processor differences in development infrastructure
  - Support for media applications
  - Off-the-shelf, optimized software components increasingly important

© 2003 Berkeley Design Technology, Inc.

41



### For More Information...

[www.BDTI.com](http://www.BDTI.com)

#### Free Information

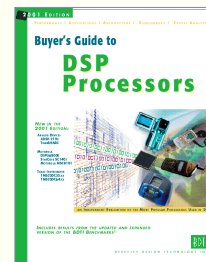
- BDTImark2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

[comp.dsp](http://comp.dsp) FAQ



2001 Edition

42

© 2003 Berkeley Design Technology, Inc.