

Alternatives to DSPs: What and Why?

Optimized DSP Software • Independent DSP Analysis



Alternatives to DSPs: What and Why?

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Presentation Goals



Why consider alternatives?
What types of alternatives are relevant?
Which companies are developing these?
What are the major distinguishing characteristics, advantages, and disadvantages of each type of alternative?



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Presented by Jeff Bier
Cambridge, UK

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May 27, 2003


Alternatives to DSPs: What and Why?




DSP Application Needs

Diverse Requirements in Many Dimensions

- Algorithms: type, complexity
 - From 10's to 10's of thousands of ops/bit
- Data rates: ~10 orders of magnitude!
- Data types: 1-D, 2-D, precision, range
- User/channel capacity
- Cost, energy, size envelope
- Flexibility
 - Multiple, evolving standards
- Market windows, product life cycles



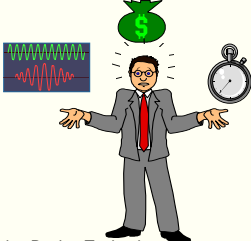
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Application Needs

Key Considerations

<ul style="list-style-type: none">Throughput, latencyEnergy efficiencySystem cost<ul style="list-style-type: none">• Chip cost• Memory use• Size and integration	<ul style="list-style-type: none">Development cost and risk<ul style="list-style-type: none">• Tools and support• Compatibility• Installed base• Roadmap• Shared vs. proprietary architecture
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In varying combinations, with diverse algorithms

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Alternatives to DSPs: What and Why?



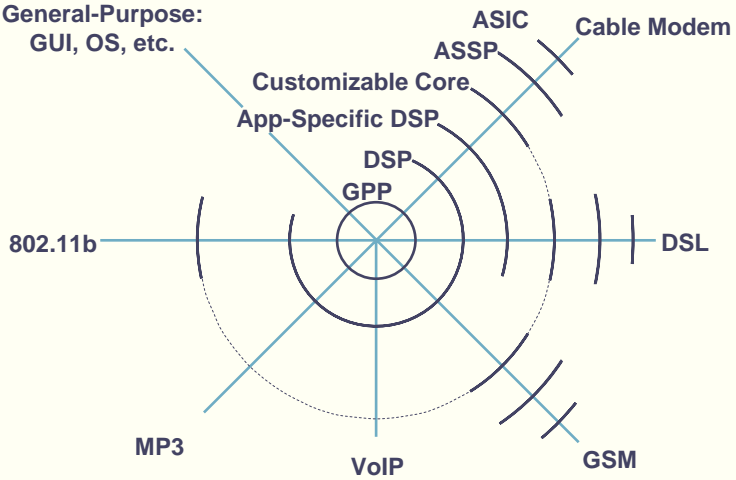
Why Consider Alternatives?

- Convergence
 - DSP-intensive products increasingly include complex non-DSP functionality
- Processing throughput, density
 - E.g., 3G wireless computation demands outstripping DSP processor advances
- Development
 - DSP processor software development infrastructure (e.g., compilers) suffers from significant limitations
- Cost
 - Desire for integration drives SoC adoption
- Energy efficiency
- Flexibility

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Flexibility vs. Suitability



General-Purpose: GUI, OS, etc.

ASIC Cable Modem

ASSP

Customizable Core

App-Specific DSP

DSP GPP

802.11b

DSL

MP3


VoIP

GSM

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Alternatives to DSPs: What and Why?



Key Alternatives


GPPs/DSP-enhanced GPPs
Media processors
Massively parallel processors
ASICs

- Licensable cores
- Customizable cores
- Platform-based design

ASSPs
Reconfigurable architectures

- FPGAs
- Reconfigurable processors

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GPPs and Hybrids


Attacking from the Top and Bottom

Today, many general-purpose processors have strong DSP capabilities

- High-performance GPPs with DSP enhancements
 - E.g., Pentium 4, PowerPC 7xxx
- Embedded GPPs with and without DSP enhancements
 - E.g., SH3-DSP, XScale

System designers often must choose between a GPP and a DSP


- Many products contain both a DSP and a GPP; eliminating one can reduce cost
- Many GPPs are adding DSP-oriented features



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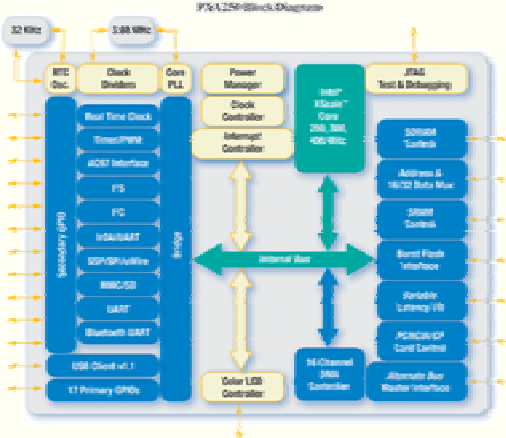
Alternatives to DSPs: What and Why?




Example: Embedded RISC CPU

PXA250

- 400 MHz, 32-bit RISC with minor DSP extensions
- BDTImark2000™ score: 930
- MPEG-4 decode (simple profile, CIF, 30 fps): 200–240 MHz
- 16-bit SIMD, 32-bit data types benefit media apps
- Predicated instruction execution good for control
- Good development tool support; optimized DSP software components available (e.g., Intel IPP)
- Price \$37.30, qty 10k



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Embedded RISC CPUs


Strengths and Weaknesses

- ↑ Can have strong DSP performance
- ↓ Dynamic features complicate programming
 - ↓ Complicates optimization & ensuring real-time behavior
- ↓ Sometimes, convoluted programming model
- Good tools, generally lack DSP support
- ↑ 32-bit GPPs better targets for non-DSP tasks
 - ↑ E.g., TCP/IP network stacks
- ↑ Multi-vendor architectures more common
- ↑ Very good 3rd-party non-DSP software component support
- ↑ Compatibility more common
- ↑ High integration parts increasingly common

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Alternatives to DSPs: What and Why?



Example: PC CPU

- VIA Technologies C3
 - 1 GHz x86 compatible
 - Moderate power consumption, cost
 - SSE support for media applications, supports fixed-, floating-point types
 - Access to massive x86 3rd-party software, tools base
 - Familiar to software, hardware developers
 - MPEG-2 decode (D1 @ 30 fps) uses 5-15% of CPU when coupled with VIA Apollo CLE266 chipset
 - Price \$39, qty 10k (C3 only)

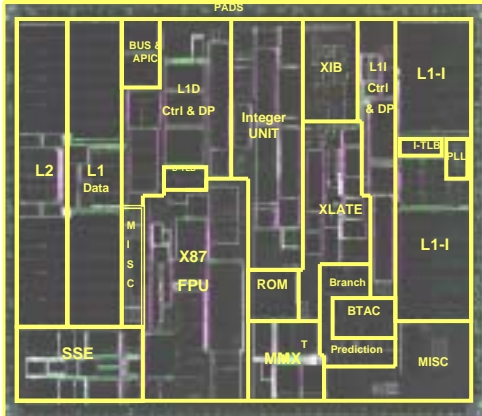



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PC CPUs (GPPs)


Strengths and Weaknesses

- ↑ High-performance GPPs can implement demanding DSP tasks
 - ↑ May be as fast or faster than DSPs...
 - ↓ ...but cost & power consumption may be higher
 - ↓ Dynamic features complicate optimization, real-time design
- ↓ Generally weak on integration
- ↓ Sometimes, convoluted programming model
- ↑ 32-bit GPPs better targets for non-DSP tasks
 - ↑ E.g., TCP/IP network stacks
- ↑ Many options for OS, 3rd party application software
- ↑ Development tools mature, powerful
 - ↓ But typically lack DSP-oriented features
- ↑ Compatibility more common

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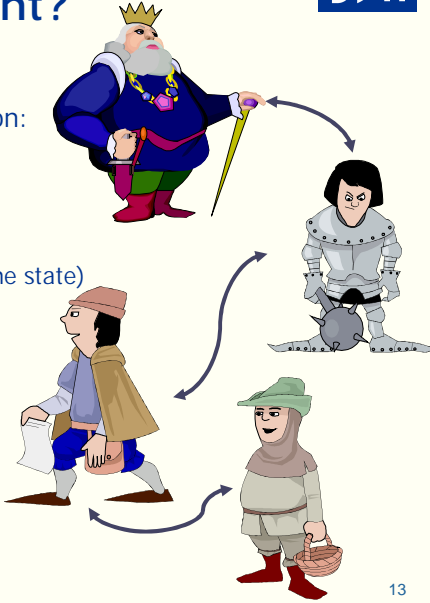
Alternatives to DSPs: What and Why?




Are Processors Efficient?

The Monarchial Model of Computing

- Steps for performing one basic operation:
 - Fetch instruction from memory
 - Decode instruction
 - Compute address
 - Fetch data
 - (Off-chip memory → L2, update cache state)
 - (L2 → L1, update cache state)
 - L1 → registers
 - Registers → arithmetic unit
 - **Perform desired operation**
 - Write result
 - All of the above in reverse order!!
 - Update data pointers
 - Update program counter



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ASICs

Chips designed for a specific end product or group of end products

Designed by the system developer


“ASIC” does not imply an architecture

- Traditionally DSP ASICs have used hard-wired logic with varied architectures
 - Sometimes with proprietary processor cores
- Increasing licensed IP content:
 - Processor cores, accelerators
 - On-chip peripherals, I/O interfaces
 - Buses
- Plus dedicated, custom logic

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Alternatives to DSPs: What and Why?




ASICs

Strengths and Weaknesses

- ↑ Offers the ultimate in tailored hardware
 - ↑ Speed, energy efficiency, cost/performance,...
 - ↑ Integration to match the product requirements
- ↓ Large development costs and risks vs. off-the-shelf hardware; mask-making costs increasing
 - ↓ Iteration is costly and time consuming
- ↓ Lengthy development cycles
 - ↓ Hardware/software integration and whole-chip verification are particularly challenging
 - ↓ Hardware/software partitioning typically must be done early
- ↓ Inflexibility
 - ↓ Long, costly development precludes frequent design changes
- ↓ Complex, costly, unreliable tools
- ↑ Vast architectural options

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Licensable Cores

At the intersection of DSPs, ASICs, ASSPs

Licensable cores have attained critical mass

Growing importance of SoCs

Growing cost of in-house processor architectures

Expanding core options

- Including customizable architectures

Licensable cores change the competitive landscape


- E.g., {LSI Logic + IBM + Broadcom} vs. TI

The recent wave of new core vendors is now receding

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Alternatives to DSPs: What and Why?



Customizable Cores

Certain features selectable by the chip designer (e.g., a 2nd MAC unit, cache)

Data path, other features often customizable

Synthesizable HDL description generated


Software tools automatically customized

A good fit for DSP applications:

- Key algorithms known and amenable to acceleration
- Computationally demanding, cost-sensitive, and/or energy-sensitive

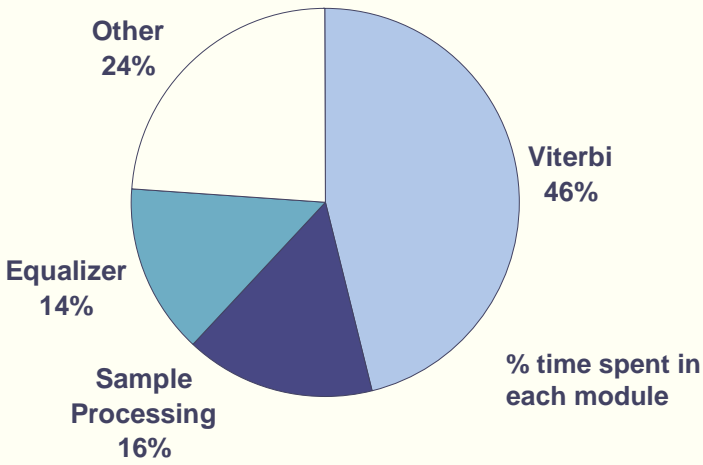
Examples: ARC, Tensilica, Improv

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Example Profile

Group III Fax Modem

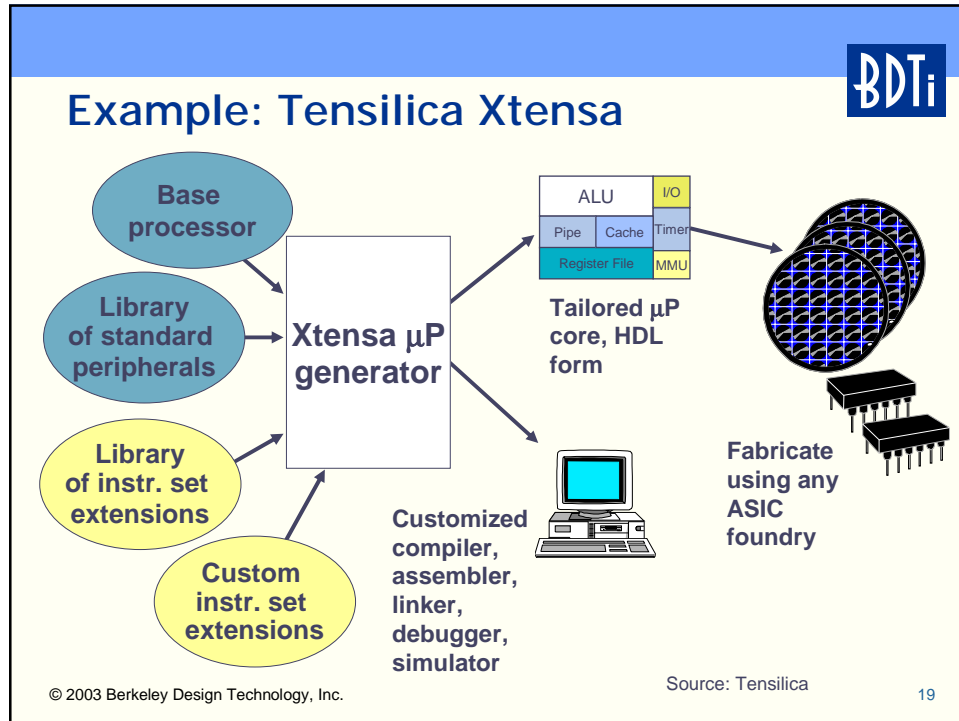


Module	% time spent
Viterbi	46%
Sample Processing	16%
Other	24%
Equalizer	14%

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Alternatives to DSPs: What and Why?



ASSPs

Application-Specific Standard Products


Off-the-shelf, fixed-function chips specialized for an application

Similar to an ASIC in design

- Many architecture possibilities
- May contain one or more processor cores
 - Which may or may not be user-programmable
- May be a SoC with memory, peripherals, special I/O, etc...
- ...or a building-block, like a video decoder

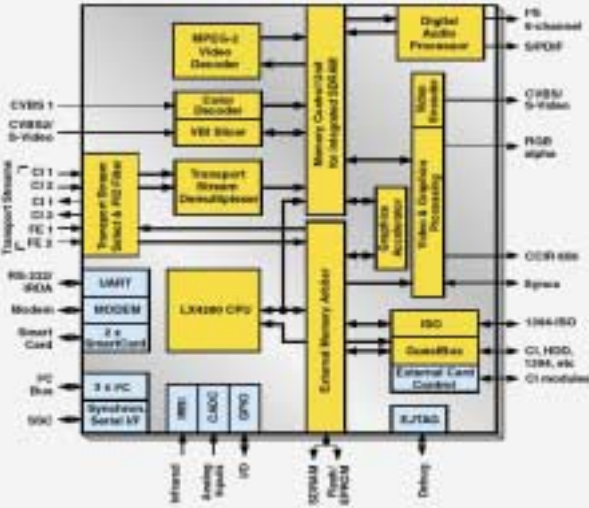
Similar to off-the-shelf processors in business model

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Example ASSP: Micronas MDE9500


- High-integration digital TV receiver
- Analog decode, DVB decryption, decode
- On-chip MPEG-2 video decoder
- Interfaces to other DTV components, VCRs, HDD
- Multi-layer software architecture
- Price not disclosed



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Alternatives to DSPs: What and Why?




ASSPs

Strengths and Weaknesses

- ↑ Often very well matched to the application
 - ↑ SoCs with extensive integration
 - ↑ Architecture tuned for the application
- ↑ Ease of use
 - ↑ Reduce system development costs
 - ↑ Reduce required implementation expertise
- ↓ Often inflexible
- ↓ Limited differentiation opportunities for system designer
- ↓ Usually single-source
- ↓ Roadmap often unclear

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FPGAs

Field-Programmable Gate Arrays

An amorphous "sea" of reconfigurable logic with reconfigurable interconnect

- Possibly interspersed with fixed-logic resources, e.g., processors, multipliers

Potential for very high parallelism

Historically used for prototyping and "glue logic," but becoming more sophisticated


- DSP-oriented architecture features
- DSP-oriented tools and design libraries
 - Viterbi, Turbo, and Reed-Solomon coders and decoders, FIR filters, FFTs,...

Key DSP players: Altera and Xilinx

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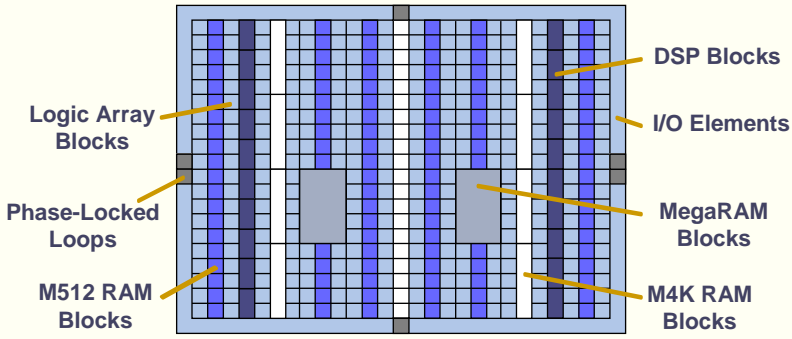


Example: Altera Stratix

Up to 28 hard-wired "DSP blocks"

- 8x9-bit, 4x18-bit, 1x36-bit multiply operations
- Optional pipelining, accumulation, etc.

Three sizes of hard-wired memory blocks



The diagram illustrates the internal architecture of an Altera Stratix FPGA. It shows a grid of Logic Array Blocks (LUTs) with various specialized blocks interspersed. On the left side, there are Phase-Locked Loops (PLLs) and M512 RAM Blocks. On the right side, there are DSP Blocks, I/O Elements, MegaRAM Blocks, and M4K RAM Blocks. Yellow arrows point from the text labels to the corresponding blocks in the diagram.

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Altera Stratix

High-end, DSP-enhanced FPGAs

IP blocks

- Filters, FFTs, Viterbi decoders,...
- Nios processor
- Third-party IP, e.g., DMA controllers

DSP tools

- Parameterized IP block generators
- Simulink-to-FPGA link
- C+ Simulink-to-FPGA design flow


Most family members available now

Prices begin at \$170 (1 ku)

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Alternatives to DSPs: What and Why?




BDTI Communications Benchmark™

	Motorola MSC8101 (300 MHz)	Altera Stratix 1S20-6 (Preliminary)	Altera Stratix 1S80-6 (Preliminary)
Channels	<<1	~10	~50
Cost (1 ku)	\$120	\$325	\$3,480
Cost per channel	~\$500	~\$10	~\$50

From BDTI's report, *FPGAs for DSP*.

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FPGAs


Strengths and Weaknesses

- ↑ Massive performance gains on some algorithms
- ↑ Architectural flexibility can yield efficiency
 - ↑ Adjust data widths throughout algorithm
 - ↑ Parallelism where you need it; distributed storage
- ↑ Re-use hardware for diverse tasks
- ↓ Slow time-to-market compared to DSPs
- ↓ Cumbersome design flow that's unfamiliar to most DSP engineers
- Suitability for single-channel, low-power, cost-sensitive DSP applications unclear

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Alternatives to DSPs: What and Why?




Summary of Alternatives

	DSPs	GPPs	FPGAs	Custom Cores	ASICs	ASSPs
Design Effort	B	A	D	C	E	A+
Design Flexibility	E	E	B	C	A	E
Run-time Flexibility	C	B	A	C	E	E
Top Speed	D	E	B	C	A	A
Energy Efficiency	C	D	C	B	A	A

A = Best, E = Worst

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Conclusions

DSPs face growing competition from many directions

- GPPs, FPGAs, licensable cores...

Software—not hardware—is often the key

- Performance advantage for DSPs over GPPs and FPGAs is diminishing
- As application complexity increases, development costs and effort shift to software
- Cutting-edge compilers and other tools are critical


There is no ideal processor

- The best processor depends on the application
- Heterogeneous solutions will become more common

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Free information

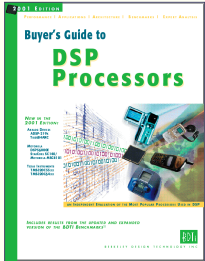
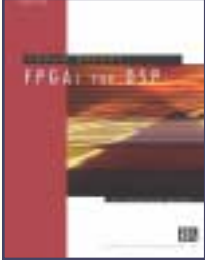
- BDTI^{mark}2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

comp.dsp FAQ



2001 Edition

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