Optimized DSP Software • Independent DSP Analysis

Comparing FPGAs and DSPs for High-Performance DSP Applications

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Application Requirements

Workload Criteria

- Computation demands
- Algorithmic parallelism
- Nature of key operations
  - E.g., control vs. signal processing
- Data precision and dynamic range
- Memory and I/O bandwidth

System constraints

- Energy consumption
- Bill of materials cost
- Integration and connectivity

Development Criteria

- Development effort and costs
- Development schedule
- Available IP
- Available skills

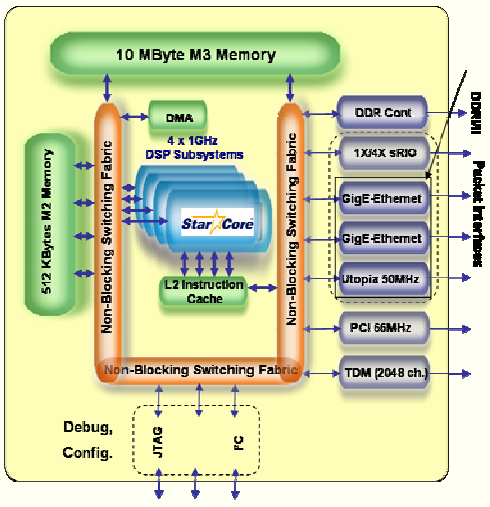
DSPs: The Incumbents

Modern conventional DSPs introduced ~1986
- One instruction, one MAC per cycle
- Developed primarily for telecom applications

High-performance VLIW DSPs introduced ~1997
- Developed primarily for wireless infrastructure
- Speed focused:
  - Independent execution units support many instructions, MACs per cycle
  - Deeper pipelines and simpler instruction sets support higher clock rates
- Emphasis on compatibility

Example: Freescale MSC8144

- 4 StarCore SC3400 16-bit DSP cores (1 GHz)
  - SC3400: high-performance VLIW architecture, 12 stage pipeline
  - I/O co-processor: 2 RISC cores (400 MHz)
  - Support for communications protocols
  - Sampling to lead customers
  - Price $233 (1 ku)



Other High-Performance DSPs

Texas Instruments TMS320C6455 (c64x+)

- 8-issue 16-bit fixed-point architecture
  - Up to eight 16-bit MACs per cycle
    - Up to two 32 x 32 MACs per cycle
  - Special instructions and co-processors for communications applications
  - Supports 16-bit as well as 32-bit instructions
- Shipping at 1 GHz, $293 (1 ku)

Picochip PC102

- Multi-core 16-bit processor array
  - 308 DSP cores (3-issue LIW , 16-bit Harvard architecture)
  - 14 co-processors and special instructions for communications
- Shipping at 160 MHz, $150 (10 ku)

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DSP Processors

Strengths and Weaknesses

- DSP performance, efficiency strong compared to other off-the-shelf processors
- But may not be adequate for demanding tasks
  - Fixed architectures limit flexibility
  - Centralized computation and extensive indirection reduce efficiency
- Relatively limited choice of chips
- But products offer strong, relevant integration

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DSP Processors

Strengths and Weaknesses

- Relatively low development cost, risk
  - Mature technology
  - Large, experienced developer base
  - Fast time-to-market

  But some vendors' roadmaps are unclear

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FPGAs

Field-Programmable Gate Arrays

An amorphous "sea" of reconfigurable logic with reconfigurable interconnect

- Typically interspersed with fixed-logic resources, e.g., memories, multipliers

Potential for very high parallelism

Historically used for prototyping and "glue logic," but becoming more sophisticated

- DSP-oriented architecture features
- DSP-oriented tools and design libraries
  - Communications oriented: Viterbi, Turbo, FFT, FIRs
  - Image and video-oriented: color space conversion, scaler, ...

Key DSP players: Altera and Xilinx

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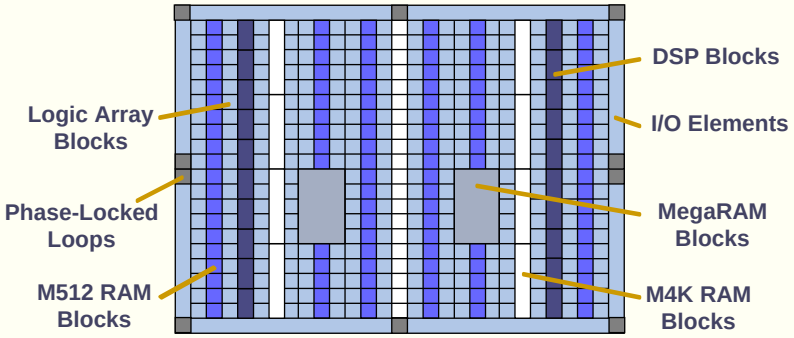
Example: Altera Stratix II

Includes array of "DSP Blocks"
- 8x9-bit, 4x18-bit, 1x36-bit multiply operations
- Optional pipelining, accumulation, etc.

Three sizes of hard-wired memory blocks



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Altera Stratix II

High-end, DSP-enhanced FPGAs

IP blocks
- Filters, FFTs, Viterbi decoders, de-interlacer…
- Nios II processor
- Third-party IP, e.g., DMA controllers

DSP tools
- Parameterized IP block generators
- Simulink to FPGA link
- C+Simulink to FPGA design flow
- C to Nios II hardware accelerator

HardCopy II
- Allows migration to pin-compatible ASICs

Most family members available now

Prices range from $55 - 912 (1 ku)

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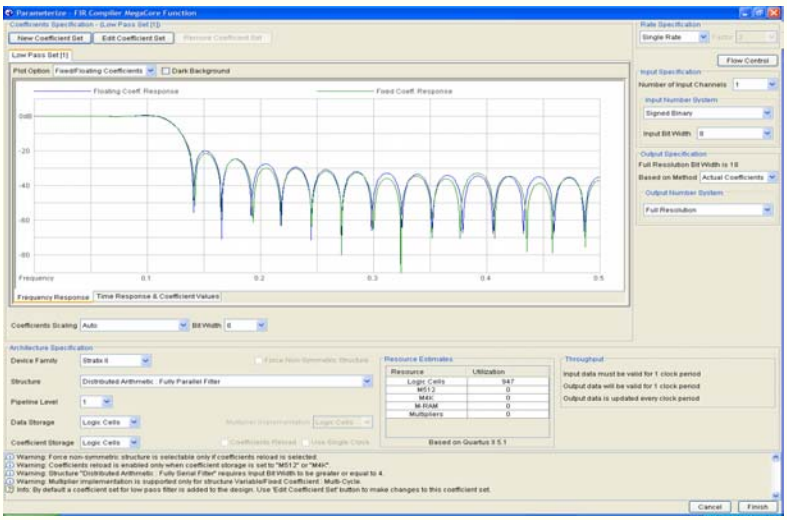
Altera FIR Filter Compiler



Source: Altera

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Others: Xilinx

"Virtex" line of FPGAs

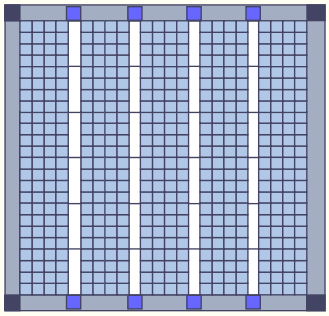
Virtex-4

- Includes array of "DSP48 Slices"
  - Hard-wired DSP data path block with 18x18 multiplier and support for various arithmetic through selection of opcodes
- Up to 192 DSP48 Slices
- Some chips in volume production

Prices begin at $89 (1 ku) for SX family devices

Virtex-5 (65 nm)

- New interconnect fabric
- Enhanced "DSP48E" data paths
  - Increased multiplier precision (25x18)
  - Support for bit-wise logical operations
- Up to 192 DSP48E Slices
- Initial products sampling now
- Prices TBD



Source: Xilinx

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FPGAs

Strengths and Weaknesses

- ↑ Massive performance gains on demanding, parallelizable algorithms
- ↑ Architectural flexibility can yield efficiency
  - ↑ Adjust data widths throughout algorithm
  - ↑ Parallelism where you need it
  - ↑ Massive on-chip memory bandwidth
  - ↑ Potential energy gains due to higher integration and exploitation of parallelism
- ↓ Efficiency compromised by generality
  - Embedded MAC units and memory blocks improve efficiency but reduce generality
- ↑ Field reconfigurability (for some products)

FPGAs

Strengths and Weaknesses

- ↑ Good cost/performance on demanding, parallelizable algorithms
- ↑ Potentially good energy efficiency on demanding, parallelizable algorithms
- ↓ Development is long and complicated
  - ↓ Higher complexity inherent due to flexibility
  - ↓ Design flow is unfamiliar to most DSP engineers
  - ↑ But development cost and complexity is much lower than ASICs'
- ↓ Development infrastructure still lags DSPs'
- ↑ Xilinx and Altera have mature products

Performance Analysis

- Comparing performance of off-the-shelf DSPs to that of FPGAs is tricky
- Common MMACS metric is oversimplified to the point of absurdity
  - FPGAs vendors use distributed-arithmetic benchmark implementations that require fixed coefficients
  - MMACS metric overlooks need to dedicate resources to non-MAC tasks
  - Many important DSP algorithms don't use MACs at all!

Alternative Approach: Application Benchmarks

Use a full application, e.g., N channels of an OFDM receiver

Hazards:

- Applications tend to be ill-defined
- Hand-optimization usually required in real-world applications
  - Costly, time-consuming to implement
  - Evaluates programmer as much as processor
  - What is a "reasonable" benchmark implementation?

Solution: Simplified Application Benchmark

BDTI's benchmark is based on a simplified OFDM receiver

- Closely resembles a real-world application
- Simplified to enable optimized implementations
- Constrained to ensure consistent, reasonable implementation practices

Benchmark goals: (two choices)

- Maximize the number of channels
- Minimize the cost per channel

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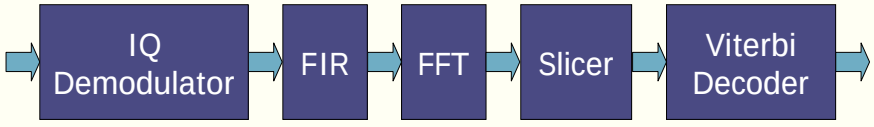
Benchmark Overview

Flexibility is an asset:

- Algorithms range from table look-ups to MAC-intensive transforms
- Data sizes range from 4 to 16 bits
- Data rates range from 40 to 320 MB/s
- Data includes real and complex values



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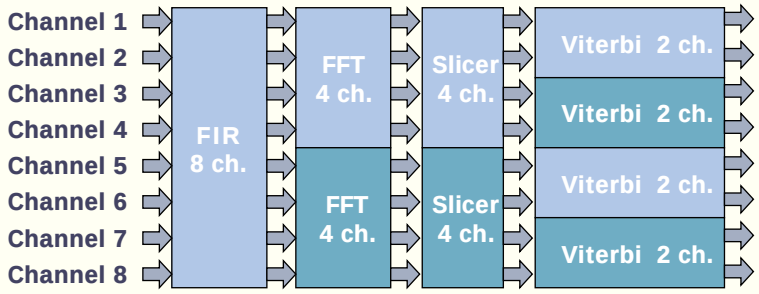
Benchmark Requirements

"Pins to pins"

Real-time throughput

Bit-exact output data

Resource sharing is permitted



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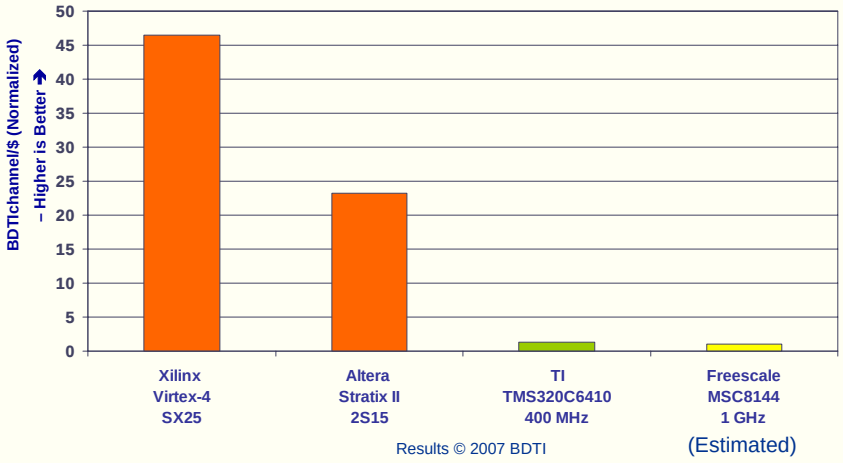
BDTI Communications Benchmark (OFDM)™

New BDTI-Certified Cost-Performance Optimized Results



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Why Use a DSP?

- Many applications are not amenable to efficient FPGA implementations
  - Parallelism is sometimes inherently limited
  - Ultimate speed is not always the first priority
- Many skilled engineers with DSP processor expertise
- Still easier to use
  - More familiar paradigm
  - Lots of in-house and third-party IP
  - Strong tools

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Conclusions

High-end FPGAs can outstrip DSPs on certain DSP tasks
- Computation-intensive, highly parallelizable tasks

High-end FPGAs can beat DSPs in terms of performance per dollar on these tasks

DSP have the advantage in development infrastructure, time-to-market, developer familiarity

In many applications, a heterogeneous combination of computing engines is desirable
- Expect to see more heterogeneous processor chips

The “best” architecture depends on the details of the application

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For More Information...

www.BDTI.com

Inside [DSP] newsletter and website

Benchmark scores for dozens of processors

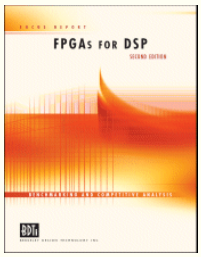
Pocket Guide to Processors for DSP

- Basic stats on over 40 processors

Articles, white papers, and presentation slides

- Processor architectures and performance
- Signal processing applications
- Signal processing software optimization

comp.dsp FAQ



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